FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. SP018.C4	APPLICATION NO. 09/188,708
	APPLICANT Garg *et al.*	
	FILING DATE November 10, 1998	GROUP 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	4,212,076	07/1980	Conners	364	706	
	AB1	5,125,092	06/1992	Prener	395	725	
	AC1	5,201,056	04/1993	Daniel *et al.*	395	800	
	AD1	5,241,636	08/1993	Kohn	395	375	
	AE1	5,487,156	01/1996	Popescu *et al.*	395	375	
	AF1	5,493,687	02/1996	Garg *et al.*	395	800.23	
	AG1	5,560,035	09/1996	Garg *et al.*	395	800.23	
	AH1	5,682,546	10/1997	Garg *et al.*	395	800.23	
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1	0 170 284	02/1986	EP			Yes No
	AM1	0 213 843	03/1987	EP			Yes No
	AN1	0 241 909	10/1987	EP			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	1	Patterson *et al.*, "A VLSI RISC," *IEEE Computer*, vol. 15, no. 9, pp. 8-18, September 1982.
	AS	1	Maejima *et al.*, "A 16-bit Microprocessor with Multi-Register Bank Architecture," *Proc. Fall Joint Computer Conference*, Nov. 2-6, 1986, pp. 1014-1019.
	AT	1	Birman *et al.*, "Design of a High-Speed Arithmetic Datapath," *IEEE*, pp. 214-216, 1988.
	AU	1	Ruby B. Lee, "Precision Architecture," *IEEE Computer*, pp. 78-91, January 1989.

EXAMINER	LARRY D. DONAGHUE PRIMARY EXAMINER	DATE CONSIDERED	11/16/99

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
✓	AL2	0 454 636	10/1991	EP			Yes / No
✓	AM2	2 190 521	11/1987	GB			Yes / No
	AN						Yes / No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

✓	AR	2	Molnar *et al.*, "Floating-Point Processors," *IEEE Intl. Solid-State Circuits Conf.*, pp. 48-49, plus Figure 1, Feb. 1989.
✓	AS	2	Steven *et al.*, "Harp: A Parallel Pipelined RISC Processor," *Microprocessors and Microsystems*, vol. 13, no. 9, pp. 579-586, Nov. 1989.
✓	AT	2	Groves *et al.*, "An IBM Second Generation RISC Processor Architecture," *35th IEEE Computer Society International Conference*, Feb. 26, 1990, pp. 166-172.
✓	AU	2	Miller *et al.*, "Exploiting Large Register Sets," *Microprocessors and Microsystems*, vol. 14, no. 6, July 1990, pp. 333-340.

EXAMINER LARRY D. DONAGHUE PRIMARY EXAMINER DATE CONSIDERED 11/16/99

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

✓	AR	3	Adams *et al.*, "Utilizing Low Level Parallelism in General Purpose Code: The HARP Project," *Micrprocessing and Microprogramming*, vol. 29, no. 3, Oct. 1990, pp. 137-149.
	AS	3	Daryl Odnert *et al.*, "Architecture and Computer Enhancements for PA-RISC Workstations," *Proc. from IEEE Compcon*, San Francisco, CA, pp. 214-218, feb. 1991.
	AT	3	Colin Hunter, "*Series 3200 Programmer's Reference Manual*," Prentice-Hall Inc., Englewood Cliffs, NJ, 1987, pp. 2-4, 2-21, 2-23, 6-14, and 6-126.
	AU		

EXAMINER	LARRY D. DONAGHUE PRIMARY EXAMINER	DATE CONSIDERED	11/16/99

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FORM PTO-1449

1ST SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
SP015.C4	09/188,708
APPLICANT: Garg *et al.*	
FILING DATE: November 10, 1998	GROUP: 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	4,626,989	12/1986	Torii	364	200	
	AB4	4,675,806	06/1987	Uchida	364	200	
	AC4	4,722,049	01/1988	Lahti	364	200	
	AD4	4,807,115	02/1989	Torng	364	200	
	AE4	5,226,126	07/1993	McFarland *et al.*	395	375	
	AF4	5,230,068	07/1993	Van Dyke *et al.*	395	375	
	AG4	5,442,757	08/1995	McFarland *et al.*	395	375	
	AH4	5,487,156	01/1996	Popescu *et al.*	395	375	
	AI4	5,561,776	10/1996	Popescu *et al.*	395	375	
	AJ4	5,592,636	01/1997	Popescu *et al.*	395	586	
	AK4	5,625,837	04/1997	Popescu *et al.*	395	800	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR ✓	4	Smith *et al.*, "Implementation of Precise Interrupts in Pipelined Processors," *Proceedings of the 12th Annual International Symposium on Computer Architecture*, June 1985, pp. 36-44.
	AS ✓	4	Wedig, R.G., Detection of Concurrency In Directly Executed Language Instruction Streams, (Dissertation), June 1982, pp. 1-179.
	AT ✓	4	Agerwala *et al.*, "High Performance Reduced Instruction Set Processors," IBM Research Division, March 31, 1987, pp. 1-61.
	AU ✓	4	Gross *et al.*, "Optimizing Delayed Branches," *Proceedings of the 5th Annual Workshop on Microprogramming*, October 5-7, 1982, pp. 114-120.

EXAMINER: LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED: 11/14/99

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5	5,627,983	05/1997	Popescu *et al.*	395	393	
	AB5	5,708,841	01/1998	Popescu *et al.*	355	800	
	AC5	5,768,575	06/1998	McFarland *et al.*	395	569	
	AD5	5,797,025	08/1998	Popescu *et al.*	395	800	
	AE5	5,832,293	11/1998	Popescu *et al.*	395	800.23	08/1997
	AF5	5,838,986	11/1998	Garg *et al.*	395	800.23	09/1997
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR ✓	5	Tjaden *et al.*, "Representation of Concurrency with Ordering Matrices," *IEEE Trans. On Computers*, Vol. C-22, No. 8, August 1973, pp. 752-761.
	AS ✓	5 ✓	Tjaden, Representation and Detection of Concurrency Using Ordering Matrices, (Dissertation), 1972, pp. 1-199.
	AT	5 ✓	Foster *et al.*, "Percolation of Code to Enhance Parallel Dispatching and Execution," *IEEE Trans. On Computers*, December 1971, pp. 1411-1415.
	AU	5 ✓	Thornton, J.E., Design of a Computer: The Control Data 6600, Control Data Corporation, 1970, pp. 58-140.

EXAMINER	LARRY D. DONAGHUE PRIMARY EXAMINER	DATE CONSIDERED 11/16/05

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	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	6	Weiss *et al.*, "Instruction Issue Logic in Pipelined Supercomputers," Reprinted from *IEEE Trans. on Computers*, Vol. C-33, No. 11, November 1984, pp. 1013-1022.
	AS	6	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," *IBM Journal*, Vol. 11, January 1967, pp. 25-33.
	AT	6	Tjaden *et al.*, "Detection and Parallel Execution of Independent Instructions," *IEEE Trans. On Computers*, Vol. C-19, No. 10, October 1970, pp. 889-895.
	AU	6	Smith *et al.*, "Limits on Multiple Instruction Issue," *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, April 1989, pp. 290-302.

EXAMINER	LARRY D. DONAGHUE PRIMARY EXAMINER	DATE CONSIDERED	11/16/01

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR ✓	Z	Pleszkun *et al.*, "The Performance Potential of Multiple Functional Unit Processors," *Proceedings of the 15th Annual Symposium on Computer Architecture*, June 1988, pp. 37-44.
	AS ✓	Z	Pleszkun *et al.*, "WISQ: A Restartable Architecture Using Queues," *Proceedings of the 14th International Symposium on Computer Architecture*, June 1987, pp. 290-299.
	AT ✓	Z	Patt *et al.*, "Critical Issues Regarding HPS, A High Performance Microarchitecture," *Proceedings of the 18th Annual Workshop on Microprogramming*, December 1985, pp. 109-116.
	AU ✓	Z	Hwu *et al.*, "Checkpoint Repair for High-Peformance Out-of-Order Execution Machines," *IEEE Trans. On Computers*, Vol. C-36, No. 12, December 1987, pp. 1496-1514.

EXAMINER	LARRY D. DONAGHUE PRIMARY EXAMINER	DATE CONSIDERED	12/16/99

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	✓ AR	8	Patt *et al.*, "HPS, A New Microarchitecture: Rationale and Introduction," *Proceedings of the 18th Annual Workshop on Microprogramming*, December 1985, pp. 103-108.
	✓ AS	8	Keller, R.M., "Look-Ahead Processors," *Computing Surveys*, Vol. 7, No. 4, December 1975, pp. 177-195.
	✓ AT	8	Jouppi *et al.*, "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, April 1989, pp. 272-282.
	✓ AU	8	Hwu *et al.*, "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality," *Proceedings from ISCA-13*, Tokyo, Japan, June 2-5, 1986, pp. 297-306.

EXAMINER LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED 11/16/01

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	✓ AR	9	Hwu *et al.*, "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," *Proceedings of the 15th Annual Symposium on Computer Architecture*, June 1988, pp. 45-53.
	✓ AS	9	Colwell *et al.*, "A VLIW Architecture for a Trace Scheduling Compiler," *Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems*, October 1987, pp. 180-192.
	✓ AT	9	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," *Proceedings of the 19th Annual Hawaii International Conference on System Sciences*, 1986, pp. 41-50.
	✓ AU	9	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," *Computer*, Vol. 14, September 1981, pp. 18-27.

EXAMINER	LARRY D. DONAGHUE PRIMARY EXAMINER	DATE CONSIDERED	11/16/99

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	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR ✓	10	Acosta, Ramón D. *et al.*, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," *IEEE Transactions On Computers*, Vol. C-35, No. 9, September 1986, pp. 815-828.
	AS ✓	10	Johnson, William M., Super-Scalar Processor Design, (Dissertation), Copyright 1989, 134 pages.
	AT ✓	10	Sohi, Gurindar S. and Sriram Vajapeyam, "Instruction Issue Logic For High-Performance, Interruptable Pipelined Processors," *Conference Proceedings of the 14th Annual International Symposium on Computer Architecture*, June 2-5, 1987, pp. 27-34.
	AU		

EXAMINER LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED 11/16/98

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	11	Smith, M.D. *et al.*, "Boosting Beyond Static Scheduling in a Superscalar Processor," *IEEE*, 1990, pp. 344-354.
	AS	11	Murakami, K. *et al.*, "SIMP (Single Instruction stream/Multiple instruction Pipelining): A Novel High-Speed Single-Processor Architecture," *ACM*, 1989, pp. 78-85.
	AT	11	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," *IEEE Transactions on Computers*, Vol. 38, No. 12, December 1989, pp. 1645-1658.
	AU	11	Horst, R.W. *et al.*, "Multiple Instruction Issue in the NonStop Cyclone Processor," *IEEE*, 1990, pp. 216-226.

EXAMINER	LARRY D. DONAGHUE PRIMARY EXAMINER	DATE CONSIDERED	11/16/99

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	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	12	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," *ACM*, 1988, pp. 442-452.
	AS	12	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," *Annu. Rev. Comput. Sci.*, Vol. 4, 1990, pp. 173-201.
	AT	12	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique*," pp. 221-235.
	AU	12	Jouppi, N.H., "Integration and Packaging Plateaus of Processor Performance," *IEEE*, 1989, pp. 229-232.

EXAMINER	LARRY D. DONAGHUE ~~PRIMARY EXAMINER~~	DATE CONSIDERED	11/16/01

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL						Yes No
	AM						Yes No
	AN						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	13	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," *IEEE*, 1989, pp. 134-137.
	AS		
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EXAMINER	DATE CONSIDERED

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

P	AR	1	*IBM Journal of Research and Development*, Vol. 34, No. 1, January 1990, pp. 1-70.
	AS	1	
	AT	1	

EXAMINER: LARRY D. DONAGHUE PRIMARY EXAMINER

DATE CONSIDERED: 11/16/99

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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